In the Specification:

Delete the paragraph starting on line 5, page 7, and replace it with the following:

In one preferred embodiment, the SOI layer 10, 12 15 could have a thickness of approximately 400nm. The collector 14 implant 19 preferably has a dose of $1x10^{16}cm^{-2}$ at a power of 1M3V. This doping profile (and other similar doping profiles that would be known by those ordinarily skilled in the art given this disclosure) produces a buried collector 14 centered at approximately the back interface of the silicon 15 and insulator or 12 layers with a peak concentration of approximately $3x10^{19}cm^{-3}$.

In the Claims:

Cancel claim 6.

Amend the following claims:

1. (Amended) A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate having a collector layer and a base layer over said collector layer;

forming a patterned mask over said base layer; and

filling openings in said mask with emitter material in a damascene process, said emitter material contacting the substrate.

5. (Amended) The method in claim 2, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

7. (Amended) The method in claim 11, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

10. (Amended) The method in claim 7, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

11. (Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

forming a gate oxide layer over only said CMOS region of said SOI substrate;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

12. (Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

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13. (Amended) The method in claim 14, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

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14. (Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors. wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

16. (Amended) The method in claim 13, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

17. (Amended) The method in claim 14, further comprising, before said forming of said polysilicon, forming a gate oxide layer over only said CMOS region of said SOI substrate.

Please add the following new claims:

18. A method of forming a bipolar device on a SOI substrate having a buried insulator layer that forms an interface with an overlying semiconductor layer, comprising the steps of:

forming in said semiconductor layer a buried collector region contered at approximately said interface; and

forming in said semiconductor layer a base region vertically stacked on said buried collector region.

19. The method of claim 18, wherein said buried collector region and said base region are